CERTIFICATE

I, the undersigned, Takashi KISO, residing at 5th Floor, Shintoshicenter Bldg., 24-1, Tsurumaki 1-chome, Tama-shi, Tokyo 206-0034 Japan, hereby certify that to the best of my knowledge and belief the following is a true translation into English made by me of Japanese Patent Application No. H11-164055 filed on June 10, 1999.

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[TITLE OF THE INVENTION] INTERLEAVE APPARATUS AND INTERLEAVE METHOD

[WHAT IS CLAIMED IS:]

[Claim 1] An interleave apparatus comprising: conversion series creating means for creating at least one sequence conversion series using any element included in a sequence conversion rule expression stipulated for every input data item; and sequence changing means for changing the sequence of the input data using the created sequence conversion series.

[Claim 2] The interleave apparatus according to claim 1, wherein the sequence changing means further comprises a first sequence calculating means for calculating the sequence of the changed sequence of the input data and changes the sequence of the input data according to the calculated sequence.

[Claim 3] The interleave apparatus according to claim 1, wherein the sequence changing means further comprises a second sequence calculating means for calculating the sequence of the input data to be placed in this input data and changes the sequence of the input data according to the calculated sequence.

[Claim 4] The interleave apparatus according to any of claims 1 through 3, wherein the conversion series creating means creates a sequence conversion series, when one element included in the sequence conversion rule expression is lower than the other element included in the sequence conversion rule expression by at least 1 stage, using the other element.

[Claim 5] The interleave apparatus according to any of claims 1 through 4, wherein the sequence changing means changes the sequence of the input data whose sequence has been changed according to the sequence conversion rule expression.

[Claim 6] A communication terminal apparatus comprising an interleave

apparatus according to any of claims 1 through 5.

[Claim 7] A base station apparatus comprising an interleave apparatus according to any of claims 1 through 5.

[Claim 8] A radio communication system which performs communication between the communication terminal apparatus according to claim 6 and the base station apparatus according to claim 7.

[Claim 9] An interleave method comprising: a conversion series creating step of creating at least one sequence conversion series using any element included in a sequence conversion rule expression stipulated for every input data item; and a sequence changing step of changing the sequence of the input data using the created sequence conversion series.

[Claim 10] An interleave method comprising: a conversion series creating step of creating at least one sequence conversion series using any element included in a sequence conversion rule expression stipulated for every input data item; and a sequence restoring step of restoring the sequence of the input data whose sequence has been changed according to said sequence conversion rule expression using the created sequence conversion series.

[DETAILED DESCRIPTION OF THE INVENTION]

【0001】

[TECHNICAL FIELD OF THE INVENTION]

The present invention relates to a coding/decoding processing apparatus and a coding/decoding processing method in a CDMA (Code Division Multiple Access) mobile communication.

【0002】

[PRIOR ART]

In order to avoid deterioration of communication quality due to burst errors on transmission paths, conventional CDMA-based communication systems use interleave that can convert burst errors to random errors by rearranging the

sequence of transmission data. Interleave (hereinafter referred to as "IL") is a technique by which an apparatus on the transmitting side transmits transmission data whose sequence has been rearranged according to a predetermined pattern and an apparatus on the receiving side restores the original sequence of the received data. This makes it possible to convert burst errors that occur on a transmission path to random errors and carry out higher-level error correction decoding.

【0003】

IL processing by the apparatus on the transmitting side is carried out using the procedure described below. Here, a case where IL processing is carried out on L data items will be explained as an example. That is, firstly an M×N matrix is created by repeating M times processing of writing N of L data items sequentially in the horizontal direction. Then, repeating N times processing of reading M data items sequentially from the matrix created in this way in the vertical direction produces L data items whose data sequence has been rearranged. This IL processing is generally expressed as L[M×N].

【0004】

In a communication system according to a next-generation mobile communication system, whose service will start from 2001, that is, a W-CDMA-based communication system, Multistage Interleave (MIL) is used as interleave. MIL is a newly proposed technique to assist higher-level error correction decoding instead of IL and used to repeat IL processing in a hierarchical fashion according to the MIL system specified for every channel that carries out communication. Hereinafter, MIL processing used in a conventional CDMA communication system will be explained. Here, a MIL expression that is expressed in the following expression will be explained as an example.

【0005】

$$20[5[3\times2]\times4[2\times2]] \quad -\ (1)$$

Expression (1) indicates that 20 input data items In[x] (x=0 to 19) (e.g., 20 data items each having address {0,1, 2, ..., 18, 19}) are developed into a 5×4 matrix, then IL processing of 4[2×2] is carried out on every row and IL processing of 5[3×2] is carried out on every row. Performing such processing develops expression (1) and produces 20 output data items Out[y] (y=0 to 19) whose sequence has been rearranged. That is, input data is written to output data sequentially according to the address shown in the following expression:

{0, 8, 16, 4, 12, 2, 10, 18, 6, 14, 1, 9, 17, 5, 13, 3, 11, 19, 7, 15} — (2)

Each number in expression (2) denotes an address.

【0006】

Here, the MIL expression expressed in a form like 5[3×2] and 4[2×2] is referred to as "MIL expression of stage 1" and the MIL expression expressed in a form like 20[5[3×2]×4[2×2]] is referred to as "MIL expression of stage 2".

【0007】

Since IL processing needs to be carried out repeatedly in the MIL processing above, using a MIL expression of a deeper stage requires longer processing time. Thus, in the conventional CDMA system, MIL processing is carried out using the MIL apparatus shown in FIG 15 to reduce processing time.

【0008】

FIG 15 is a block diagram showing a configuration of a conventional MIL apparatus. As shown in FIG 15, the conventional MIL apparatus is configured by input memory 1501, memory reading/writing apparatus 1502, output memory 1503 and MIL pattern memory 1504 that stores MIL patterns.

【0009】

In the MIL apparatus shown in FIG 15, MIL pattern memory 1504 stores a MIL pattern of stage 0 created from the MIL expression and memory reading/writing apparatus 1502 performs indirect addressing on the stored MIL

pattern, and thereby the sequence of transmission data can be rearranged. Here, the operation of the MIL apparatus shown in FIG 15 will be explained below by taking a case where the MIL expression shown in expression (1) is used as an example.

【0010】

As described above, developing the MIL expression shown in expression (1) produces a MIL pattern shown in expression (2). This MIL pattern is stored in MIL pattern memory 1504 in FIG 15. Furthermore, 20 input data items In[x] (x=0 to 19) (e.g., 20 data items each having address {0,1, 2, ..., 18, 19}) are stored in input memory 1501. Suppose the data items stored in input memory 1501, output memory 1503 and MIL pattern memory 1504 of FIG 15 are In[x], Out[y] and Mil[z] (x, y, z=0 to 19), respectively. Then, MIL processing is carried out according to an operation flow shown in FIG 16.

【0011】

FIG 16 is a flow chart showing the operation of the conventional MIL apparatus. As shown in FIG 16, memory reading/writing apparatus 1502 accesses memory 1501 sequentially according to the addresses shown in expression (2) and writes the accessed data in output memory 1503, and thereby the output data whose sequence of the input data stored in input memory 1501 is rearranged is written in output memory 1503. According to such MIL processing, the processing time is not affected by the depth of stage of the MIL expression used, and therefore the processing time is shortened.

[PROBLEMS TO BE SOLVED BY THE INVENTION]

However, MIL pattern memory 1504 of the conventional MIL apparatus above stores data equivalent in size to the input data to be subjected to MIL processing. Accordingly the conventional MIL apparatus involves a problem that as the amount of input data (number of bits) increases, the amount of memory required grows a great deal.

The present invention has been made in view of the foregoing, aiming to provide an interleave apparatus that reduces the amount of memory required.

【0012】

[MEANS FOR SOLVING THE PROBLEMS]

This essence of the present invention is to create at least one MIL pattern (sequence conversion series) using any element included in a MIL expression (sequence conversion rule expression) stipulated or specified for every input data item, thereby changing the sequence of the input data using the created MIL pattern.

【0013】

[DESCRIPTION OF THE SPECIAL EMBODIMENTS]

The apparatus according to the first embodiment of the present invention has a configuration comprising a conversion series creating section for creating at least one sequence conversion series using any element included in a sequence conversion rule expression specified for every input data item and a sequence changing section for changing the sequence of the input data using the created sequence conversion series.

【0014】

This configuration makes it possible to create a sequence conversion series (MIL pattern) using any element in the sequence conversion rule (MIL expression), for example, a row pattern expression or column pattern expression created from each element of stage 1 and change the sequence of the input data using the created sequence conversion series, and therefore allows MIL processing to be performed with a reduced amount of memory required.

【0015】

The apparatus according to the second embodiment of the present invention has a configuration with the sequence changing section of the first embodiment further comprising a first sequence calculating section for calculating the

changed sequence of the input data and changing the sequence of the input data according to the calculated sequence.

【0016】

This configuration ensures that the sequence of the input data is changed by calculating the sequence after the change of the sequence of the input data using the created sequence conversion series.

【0017】

The apparatus according to the third embodiment of the present invention has a configuration with the sequence changing section of the first embodiment further comprising a second sequence calculating section for calculating the sequence of input data to be placed in this input data and changing the sequence of the input data according to the calculated sequence.

【0018】

This configuration ensures that the sequence of the input data is changed by calculating the sequence of the input data to be placed in the input data after the change of the sequence using the created sequence conversion series.

【0019】

The apparatus according to the fourth embodiment of the present invention has a configuration with the conversion series creating section of any one of the first embodiment to third embodiment creating a sequence conversion series, when one element included in the sequence conversion rule expression is lower than the other element by at least 1 stage, using the other element.

【0020】

This configuration allows the amount of required memory to be further reduced by creating a sequence conversion series using only a column pattern expression when, for example, only the column pattern expression is included in the sequence conversion rule expression.

【0021】

The apparatus according to the fifth embodiment of the present invention has a configuration with the sequence changing section of the first embodiment to fourth embodiment changing the sequence of input data whose sequence has been changed according the sequence conversion rule expression.

【0022】

This configuration allows the original sequence of the input data whose sequence has been changed according to this sequence conversion rule expression to be restored by using the sequence conversion series created using the same sequence conversion rule expression.

【0023】

A communication terminal apparatus according to Embodiment 6 of the present invention comprises the interleave apparatus according to any of Embodiments 1 through 5.

【0024】

This configuration provides a communication terminal apparatus with a reduced circuit scale by including an interleave apparatus that reduces required memory.

【0025】

A base station apparatus according to Embodiment 7 of the present invention comprises the interleave apparatus according to any of Embodiments 1 through 5.

【0026】

This configuration provides a base station apparatus with a reduced circuit scale by including an interleave apparatus that reduces required memory.

【0027】

A radio communication system according to Embodiment 8 of the present invention performs communication between a communication terminal apparatus according to Embodiment 6 and a base station apparatus according to Embodiment 7.

【0028】

This configuration allows efficient radio communications to be implemented using the communication terminal apparatus and base station apparatus with a reduced circuit scale.

【0029】

The method according to the ninth embodiment of the present invention comprises a conversion series creating step of creating at least one sequence conversion series using any element included in a sequence conversion rule expression specified for every input data item and a sequence changing step of changing the sequence of the input data using the created sequence conversion series.

【0030】

This method makes it possible to create a sequence conversion series using any elements in the sequence conversion rule, for example, a row pattern expression or column pattern expression created from each element of stage 1 and change the sequence of the input data using the created sequence conversion series, and therefore allows MIL processing to be performed with a reduced amount of memory required.

【0031】

The method according to the ninth embodiment of the present invention comprises a conversion series creating step of creating at least one sequence conversion series using any element included in a sequence conversion rule expression specified for every input data item and a sequence restoring step of restoring the sequence of the input data whose sequence has been changed according to said sequence conversion rule expression using the created sequence conversion series.

【0032】

This method allows the original sequence of input data whose sequence has

been changed according to this sequence conversion rule expression to be restored by using the sequence conversion series created using the same sequence conversion rule expression.

【0033】

The following will specifically explain embodiments of the present invention with reference to the drawings.

【0034】

(Embodiment 1)

FIG 1 is a block diagram showing the configuration of an MIL apparatus according to Embodiment 1 of the present invention. The MIL apparatus according to this embodiment is an apparatus that rearranges the sequence of data in a frame. This embodiment will be explained using 20[5[3×2]×4[2×2]] shown in expression (1) as the MIL expression (sequence conversion rule expression) as an example.

【0035】

In FIG 1, input memory 101 stores 20 input data items In[x] (x=0 t 19). Here, the addresses of input data items are assumed to be {0,1,2,...,18,19}.

【0036】

Row pattern memory 102 stores a MIL pattern (sequence conversion series) created from the MIL expression (5[3×2]) of stage 1 in expression (1), that is, row pattern Mil_row[r] shown in the following expression:

Mil_row[r](r=0 to 4)={0,2,4,1,3} -(3)

【0037】

Column pattern memory 103 stores a MIL pattern (sequence conversion series) created from the MIL expression (4[2×2]) of stage 1 in expression (1), that is, column pattern Mil_col[c] shown in the following expression:

Mil_col[c](c=0 to 3)={0,2,1,3} -(4)

【0038】

Output memory 104 stores 20 output data items Out[y] (y=0 to 19) with the sequence of input data rearranged.

【0039】

Address calculation apparatus 105 calculates addresses of the input data to be written to the output data and further writes input data read from input memory 101 in output memory 104 as output data based on the calculated input addresses. Here, processing of writing to output memory 104 by address calculation apparatus 105 will be explained with reference to FIG 2. FIG 2 is a flow chart showing processing of writing to output memory 104 by address calculation apparatus 105 in the MIL apparatus according to Embodiment 1 of the present invention.

【0040】

In step (hereinafter referred to as "ST") 201, supposing c=0 first, processing up to ST205, which will be described later, is repeated and the process ends when c>C-1 is satisfied. Here, C is the number of rows (here 4).

【0041】

In ST202, supposing r=0 first, processing up to ST204, which will be described later, is repeated and the process moves on to ST205 only when r>R-1 is satisfied. Here, R is the number of rows (here 5).

【0042】

In ST203, the address of input data to be written to output data [r+R×c] is calculated as shown in the following expression:

$$Mil\_col[c]+Mil\_row[r]\times C \qquad -(5)$$

Furthermore, the input data stored at the address calculated according to expression (5) in input memory 101 is read and written in output memory 104 as output data [r+R×c].

【0043】

In ST204, after 1 is added to the value of r, the process moves on to ST202. In

ST205, after 1 is added to the value of c, the process moves on to ST201.

【0044】

Through the writing processing above by address calculation apparatus 105, the input data stored in input memory 101 is written to output data [y] (0 to 19) in output memory 104 sequentially according to the addresses shown in expression (2). That is, for example, input data [0], input data [8] and input data [16] are written to output data [0], output data [1] and output data [2], respectively.

【0045】

As shown above, when the MIL expression shown in expression (1) is used, it is possible to implement MIL processing only with memory of a total of 9 words (except input/output memory); 5 words for the row pattern memory and 4 words for the column pattern memory. The output data written to output memory 104, that is, the input data whose sequence has been rearranged by MIL processing is then subjected to predetermined CDMA-based processing and sent.

【0046】

As shown above, this embodiment stores a pattern developed from a MIL expression of stage 1 included in the MIL expression to be used, calculates the address of input data to be written for each output data item using the stored pattern and writes the input data stored at the calculated address to the output data sequentially, and therefore can implement MIL processing with a small amount of memory.

【0047】

Furthermore, this embodiment describes the case where immediately after the address of input data to be written for each output data item is calculated, the input data items stored at the calculated addresses are written one by one to the output data, but the present invention is not limited to this, and the input data stored at the calculated addresses can also be read and written to the output data

after the addresses of input data items to be written are calculated for all output data items.

【0048】

Here, the result of reduction of required memory of the MIL apparatus according to this embodiment will be explained with reference to FIG 3. FIG 3 shows the amount of memory required of the MIL apparatus according to Embodiment 1 of the present invention in comparison with the conventional system. FIG 3 shows the amounts of memory required when the following two MIL expressions are used:

① 320[16[4[2x2]x4[2x2]]x20[4[2x2]x5[3x2]]]

② 81376[5086[80[10[5[3x2]x2]x8[4[2x2]x2]]
x64[8[4[2x2]x2]x8[4[2x2]x2]]]x16[4[2x2]x4[2x2]]]

As is clear from FIG 3, this embodiment achieves a drastic reduction of the amount of memory required compared to the conventional system. Furthermore, the effect grows as the amount of data to be subjected to MIL processing increases.

【0049】

This embodiment describes the case where expression (1) is used as the MIL expression, but the present invention is also applicable to a case where a MIL expression of deeper stage is used. For example, when expression ① shown in FIG 3 is used as a MIL expression, row pattern memory 102 stores a row pattern created from MIL expression of stage 2(16[4[2x2]x4[2x2]])in expression ① and column pattern memory 103 stores a column pattern created from MIL expression of stage 2 (20[4[2x2]x5[3x2]])in expression ① and address calculation apparatus 105 calculates as described above using the patterns above.

【0050】

(Embodiment 2)

Embodiment 2 implements MIL processing by calculating the address of

output data to be written for each input data item and writing each input data item at the address calculated in the output memory in Embodiment 1.

【0051】

What this embodiment differs from Embodiment 1 is processing of writing to output memory 104 by the address calculation apparatus. Furthermore, this embodiment differs from Embodiment 1 in row patterns stored in row pattern memory 102 and column patterns stored in column pattern memory 103. The components of this embodiment with the same configuration as that of Embodiment 1 will be explained with the same reference numerals assigned. In this embodiment, as in the case of Embodiment 1, the MIL expression shown in expression (1) will be used.

【0052】

First, row pattern memory 102 stores row pattern Mil_row[r] shown in the following expression created from MIL expression (5[2×3]).

Mil_row[r](r=0 to 4)={0,3,1,4,2} -(6)

【0053】

Furthermore, column pattern memory 103 stores Mil_col[c] shown in the following expression created from MIL expression (4[2×2]).

Mil_col[c](c=0 to 3)={0,2,1,3} -(7)

【0054】

Furthermore, the address calculation apparatus calculates the addresses of output data to be written for the input data and writes the input data at the addresses calculated in output memory 104. Here, processing of writing to output memory 104 by the address calculation apparatus will be explained with reference to FIG 4. FIG 4 is a flow chart showing processing of writing to output memory 104 by address calculation apparatus in the MIL apparatus according to Embodiment 2 of the present invention.

【0055】

In ST401, supposing r=0 first, processing up to ST405, which will be described later, is repeated and the process ends when r>R-1 is satisfied. Here, R is the number of rows (here 5).

【0056】

In ST402, supposing c=0 first, processing up to ST404, which will be described later, is repeated and the process moves on to ST405 only when c>C-1 is satisfied. Here, C is the number of rows (here 4).

【0057】

In ST403, the address of output data to which input data [c+C×r] is to be written is calculated as shown in the following expression:

Mil_row[r]+Mil_col[c]×R -(8)

Furthermore, input data [c+C×r] is written at the addresses calculated according to expression (8) in output memory 104.

【0058】

In ST404, after 1 is added to the value of c, the process moves on to ST402. In ST405, after 1 is added to the value of r, the process moves on to ST401.

【0059】

Through the writing processing above by the address calculation apparatus, the input data items stored in input memory 101 are written at the addresses in output memory 104 calculated according to expression (8) sequentially.

【0060】

As shown above, when the MIL expression shown in expression (1) is used, it is possible to implement MIL processing only with memory of a total of 9 words (except input/output memory); 5 words for the row pattern memory and 4 words for the column pattern memory.

【0061】

As shown above, this embodiment stores a pattern developed from a MIL expression of stage 1 included in the MIL expression to be used, calculates the

address of output memory to be written for each input data item using the stored pattern and writes the input data at the calculated address, and therefore can implement MIL processing with a small amount of memory.

【0062】

(Embodiment 3)

Embodiment 3 implements MIL processing by writing data to output memory using addresses calculated using only column patterns in the case where the sequence of data is rearranged between frames, that is, when the column pattern is a simple incremental value in Embodiment 1.

【0063】

In a CDMA communication, data may be rearranged not only in a frame but also between frames. This is referred to as "inter-frame interleave (inter-frame MIL)". The MIL expression used for inter-frame interleave is normally expressed in a form of $L[M_1 \times N_1 [M_2 \times N_2]]$and in this MIL expression, only column pattern expression ($N_1 [M_2 \times N_2]$) exists. A description will be made below to an MIL apparatus according to the present embodiment.

【0064】

What this embodiment differs from Embodiment 1 is processing of writing to output memory 104 by the address calculation apparatus. Furthermore, in this embodiment, row pattern memory 102 in Embodiment 1 is excluded. In this embodiment, only differences from Embodiment 1 will be explained below. The components of this embodiment with the same configuration as that of Embodiment 1 will be explained with the same reference numerals assigned. In this embodiment, the MIL expression shown below will be used.

$$80[20\times4[2\times2]] \qquad -(9)$$

【0065】

First, column pattern memory 103 stores column pattern Mil_col[c] shown in the following expression created from MIL expression (4[2×2]) of stage 1 in

expression (9).

Mil_col[c](c=0 to 3)={0,2,1,3} -(10)

【0066】

Furthermore, the address calculation apparatus calculates addresses of input data to be written to output data and writes the input data read from input memory 101 based on the calculated input addresses to output memory 104 as output data. Here, processing of writing to output memory 104 by the address calculation apparatus will be explained with reference to FIG 5. FIG 5 is a flow chart showing processing of writing to output memory 104 by address calculation apparatus in the MIL apparatus according to Embodiment 3 of the present invention.

【0067】

In ST501, supposing c=0 first, processing up to ST505, which will be described later, is repeated and the process ends when c>C-1 is satisfied. Here, C is the number of rows (here 4).

【0068】

In ST502, supposing r=0 first, processing up to ST504, which will be described later, is repeated and the process moves on to ST505 only when r>R-1 is satisfied. Here, R is the number of rows (here 20).

【0069】

In ST503, the address of input data to be written to output data [r+R×c] is calculated as shown in the following expression:

r×C+Mil_col[c] -(11)

Furthermore, the input data stored at the address calculated according to expression (11) in input memory 101 is read and written in output memory 104 as output data [r+R×c].

【0070】

In ST504, after 1 is added to the value of r, the process moves on to ST502. In

ST505, after 1 is added to the value of c, the process moves on to ST501.

【0071】

Inter-frame interleave can be implemented by Embodiment 1 or Embodiment 2 above. However, since the MIL expression shown in expression (9) includes an increment value, it is necessary to store simple increment data in row pattern memory 102 when Embodiment 1 or Embodiment 2 is used. Therefore, when inter-frame interleave is performed, it is more efficient to use a MIL apparatus without row pattern memory as in this embodiment.

【0072】

Here, the following is a comparison between the conventional system and Embodiments 1 to 3 with respect to an amount of memory required to implement inter-frame interleave using the MIL expression shown in expression (9):

① Conventional system: 80 words

② Embodiment 1 and Embodiment 2: 24 words

③ Embodiment 3: 4 words

In the case of the MIL apparatus according to Embodiment 3, the amount of memory required is 1/20 of that in the conventional system and 1/6 in Embodiment 1 and Embodiment 2. Thus, with respect to inter-frame interleave, the MIL apparatus according to this embodiment is extremely effective.

【0073】

Thus, when inter-frame interleave is performed, this embodiment stores only column patterns developed from a MIL expression of stage 1 included in the MIL expression to be used, further calculates the addresses of input data items to be written for output data items and writes input data items stored at the calculated addresses sequentially, and therefore can implement MIL processing with a small amount of memory.

【0074】

(Embodiment 4)

Embodiment 4 implements MIL processing by calculating addresses of output data to be written for input data and writing the input data at the calculated addresses in the output memory when the sequence of data is rearranged between frames, that is, when a column pattern is a simple incremental value in Embodiment 2.

【0075】

What this embodiment differs from Embodiment 2 is processing of writing to output memory 104 by the address calculation apparatus. Furthermore, in this embodiment, row pattern memory 102 in Embodiment 2 is excluded. In this embodiment, only differences from Embodiment 1 will be explained below. The components of this embodiment with the same configuration as that of Embodiment 1 will be explained with the same reference numerals assigned. In this embodiment, as in the case of Embodiment 3, the MIL expression shown in expression (9) will be used.

【0076】

First, column pattern memory 103 stores column pattern Mil_col[c] shown in expression (10) as in the case of Embodiment 3. Furthermore, the address calculation apparatus calculates the addresses of output data to be written for the input data and writes the input data at the addresses calculated in output memory 104. Here, processing of writing to output memory 104 by the address calculation apparatus will be explained with reference to FIG 6. FIG 6 is a flow chart showing processing of writing to output memory 104 by address calculation apparatus in the MIL apparatus according to Embodiment 4 of the present invention.

【0077】

In ST601, supposing r=0 first, processing up to ST605, which will be described later, is repeated and the process ends when r>R-1 is satisfied. Here, R is the

number of rows (here 20).

【0078】

In ST602, supposing c=0 first, processing up to ST604, which will be described later, is repeated and the process moves on to ST605 only when c>C-1 is satisfied. Here, C is the number of rows (here 4).

【0079】

In ST603, the address of output data to which input data [c+C×r] is to be written is calculated as shown in the following expression:

r+R×Mil_col[c] -(12)

Furthermore, input data [c+C×r] is written at the addresses calculated according to expression (12) in output memory 104.

【0080】

In ST604, after 1 is added to the value of c, the process moves on to ST602. In ST605, after 1 is added to the value of r, the process moves on to ST601.

【0081】

Thus, when inter-frame interleave is performed, this embodiment stores only column patterns developed from a MIL expression of stage 1 included in the MIL expression to be used, further calculates the addresses of output data to be written for input data and writes input data at the calculated addresses, and therefore can implement MIL processing with a small amount of memory.

【0082】

(Embodiment 5)

Embodiment 5 implements a De-MIL (De-Multistage InterLeave) apparatus that restores the original sequence of data whose sequence has been rearranged by MIL processing. The De-MIL apparatus according to this embodiment can be implemented with the same configuration as that of Embodiment 1 (FIG 1). Hereinafter only differences of the De-MIL apparatus according to this embodiment from Embodiment 1 will be explained with reference to FIG 1. In

this embodiment, a case where the original sequence of data whose sequence has been rearranged according to the MIL expression shown in expression (1) is restored will be explained as an example.

【0083】

In FIG 1, input memory 101 stores 20 input data items In[x] (x=0 to 19) whose sequence has been rearranged. Row pattern memory 102 stores the row pattern shown in expression (6). Column pattern memory 103 stores the column pattern shown in expression (7). Output memory 104 stores 20 output data items Out[y] (y=0 to 19) with the original sequence of input data restored.

【0084】

Address calculation apparatus 105 calculates addresses of the input data to be written to the output data and further writes input data read from input memory 101 in output memory 104 as output data based on the calculated input addresses. Here, processing of writing to output memory 104 by address calculation apparatus 105 will be explained with reference to FIG 7. FIG 7 is a flow chart showing processing of writing to output memory 104 by address calculation apparatus 105 in the De-MIL apparatus according to Embodiment 5 of the present invention.

【0085】

In ST701, supposing r=0 first, processing up to ST705, which will be described later, is repeated and the processing ends when r>R-1 is satisfied. Here, R is the number of rows (here 5).

【0086】

In ST702, supposing c=0 first, processing up to ST704, which will be described later, is repeated and the process moves on to ST705 only when c>C-1 is satisfied. Here, C is the number of rows (here 4).

【0087】

In ST703, the address of input data to be written to output data [C×r+c] is

calculated as shown in the following expression:

Mil_row[r]+R×Mil_col[c] -(13)

Furthermore, in input memory 101, input data stored at addresses calculated according to expression (13) is read and written in output memory 104 as output data [C×r+c].

【0088】

In ST704, after 1 is added to the value of c, the process moves on to ST702. In ST705, after 1 is added to the value of r, the process moves on to ST701.

【0089】

As shown above, this embodiment stores a pattern developed from a MIL expression of stage 1 included in the MIL expression to be used, calculates the address of input data to be written for each output data item using the stored pattern and writes the input data stored at the calculated addresses to the output data sequentially, and therefore can implement De-MIL processing with a small amount of memory.

【0090】

(Embodiment 6)

Embodiment 6 implements De-MIL processing by calculating the address of output data to be written for each input data item and writing each input data item at the address calculated in the output memory in Embodiment 5.

【0091】

What this embodiment differs from Embodiment 5 is processing of writing to output memory 104 by the address calculation apparatus. Furthermore, this embodiment differs from Embodiment 5 in row patterns stored in row pattern memory 102 and column patterns stored in column pattern memory 103. The components of this embodiment with the same configuration as that of Embodiment 5 will be explained with the same reference numerals assigned. In this embodiment, as in the case of Embodiment 5, the case where the original

sequence of data whose sequence has been rearranged according to the MIL expression shown in expression (1) is restored will be explained as an example.

【0092】

First, row pattern memory 102 stores row pattern Mil_row[r] shown in expression (3) and column pattern memory 103 stores column pattern Mil_col[c] shown in expression (4).

【0093】

Furthermore, the address calculation apparatus calculates the addresses of output data to be written for the input data and writes the input data at the addresses calculated in output memory 104. Here, processing of writing to output memory 104 by the address calculation apparatus will be explained with reference to FIG 8. FIG 8 is a flow chart showing processing of writing to output memory 104 by address calculation apparatus in the De-MIL apparatus according to Embodiment 6 of the present invention.

【0094】

In ST801, supposing c=0 first, processing up to ST805, which will be described later, is repeated and the process ends when c>C-1 is satisfied. Here, C is the number of columns (here 4).

【0095】

In ST802, supposing r=0 first, processing up to ST804, which will be described later, is repeated and the process moves on to ST805 only when r>R-1 is satisfied. Here, R is the number of rows (here 5).

【0096】

In ST803, the address of output data to which input data [r+c×R] is to be written is calculated as shown in the following expression:

C×Mil_row[r]+Mil_col[c] -(14)

Furthermore, input data [r+c×R] is written at the address calculated according to expression (14) in output memory 104.

【0097】

In ST804, after 1 is added to the value of r, the process moves on to ST802. In ST805, after 1 is added to the value of c, the process moves on to ST801.

【0098】

As shown above, this embodiment stores a pattern developed from a MIL expression of stage 1 included in the MIL expression to be used, calculates the address of output memory to be written for each input data item using the stored pattern and writes the input data at the calculated address, and therefore can implement De-MIL processing with a small amount of memory.

【0099】

(Embodiment 7)

Embodiment 7 implements De-MIL processing by writing data in output memory using addresses calculated using only a column pattern when the original sequence of data is restored between frames in Embodiment 5, that is, when a column pattern is a simple incremental value.

【0100】

What this embodiment differs from Embodiment 5 first is processing of writing to output memory by the address calculation apparatus. Furthermore, in this embodiment, row pattern memory 102 in Embodiment 5 is excluded. In this embodiment, only differences from Embodiment 5 will be explained below. The components of this embodiment with the same configuration as that of Embodiment 5 will be explained with the same reference numerals assigned. In this embodiment, the case where the original sequence of data whose sequence has been rearranged according to the MIL expression shown in expression (9) is restored will be explained as an example.

【0101】

First, column pattern memory 103 stores column pattern Mil_col[c] shown in expression (10) created from MIL expression (4[2×2]) of stage 1 in expression (9).

【0102】

Furthermore, the address calculation apparatus calculates addresses of input data to be written to output data and writes the input data read from input memory 101 based on the calculated input addresses to output memory 104 as output data. Here, processing of writing to output memory 104 by the address calculation apparatus will be explained with reference to FIG 9. FIG 9 is a flow chart showing processing of writing to output memory 104 by address calculation apparatus in the De-MIL apparatus according to Embodiment 7 of the present invention.

【0103】

In ST901, supposing r=0 first, processing up to ST905, which will be described later, is repeated and the process ends when r>R-1 is satisfied. Here, R is the number of rows (here 20).

【0104】

In ST902, supposing c=0 first, processing up to ST904, which will be described later, is repeated and the process moves on to ST905 only when c>C-1 is satisfied. Here, C is the number of rows (here 4).

【0105】

In ST903, the address of input data to be written to output data [C×r+c] is calculated as shown in the following expression:

R×Mil_col[c]+r -(15)

Furthermore, in input memory 101, input data stored at addresses calculated according to expression (15) is read and written in output memory 104 as output data [C×r+c].

【0106】

In ST904, after 1 is added to the value of c, the process moves on to ST902. In ST905, after 1 is added to the value of r, the process moves on to ST901.

【0107】

As shown above, when the original sequence of data is restored between frames, this embodiment only stores a column pattern developed from a MIL expression of stage 1 included in the MIL expression to be used, calculates addresses of input data to be written for each output data item using the stored pattern and writes the input data stored at the calculated addresses to the output data sequentially, and therefore can implement De-MIL processing with a small amount of memory.

【0108】

(Embodiment 8)

Embodiment 8 implements De-MIL processing by calculating the addresses of output data to be written for each input data item using only a column pattern and writing each input data item at the calculated address in output memory when the original sequence of data is restored between frames in Embodiment 6, that is, when a column pattern is a simple incremental value.

【0109】

What this embodiment differs from Embodiment 6 is processing of writing to output memory 104 by the address calculation apparatus. Furthermore, in this embodiment, row pattern memory 102 in Embodiment 6 is excluded. In this embodiment, only differences from Embodiment 6 will be explained below. The components of this embodiment with the same configuration as that of Embodiment 1 will be explained with the same reference numerals assigned. In this embodiment, the case where the original sequence of data whose sequence has been rearranged according to the MIL expression shown in expression (9) is restored will be explained as an example.

【0110】

First, column pattern memory 103 stores column pattern Mil_col[c] shown in expression (10). Furthermore, the address calculation apparatus calculates the addresses of output data to be written for the input data and writes the input

data at the addresses calculated in output memory 104. Here, processing of writing to output memory 104 by the address calculation apparatus will be explained with reference to FIG 10. FIG 10 is a flow chart showing processing of writing to output memory 104 by address calculation apparatus in the De-MIL apparatus according to Embodiment 8 of the present invention.

【0111】

In ST1001, supposing c=0 first, processing up to ST1005, which will be described later, is repeated and the process ends when c>C-1 is satisfied. Here, C is the number of rows (here 4).

【0112】

In ST1002, supposing r=0 first, processing up to ST1004, which will be described later, is repeated and the process moves on to ST1005 only when r>R-1 is satisfied. Here, R is the number of rows (here 20).

【0113】

In ST1003, the address of output data to which input data [r+c×R] is to be written is calculated as shown in the following expression:

r+R×Mil_col[c] -(16)

Furthermore, input data [r+c×R] is written at the address calculated according to expression (16) in output memory 104.

【0114】

In ST1004, after 1 is added to the value of r, the process moves on to ST1002. In ST1005, after 1 is added to the value of c, the process moves on to ST1001.

【0115】

As shown above, when the original sequence of data is restored between frames, this embodiment only stores a column pattern developed from a MIL expression of stage 1 included in the MIL expression to be used, calculates the address in output memory in which the data is to be written using the stored pattern and writes the input data at the calculated address, and therefore can

implement De-MIL processing with a small amount of memory.

【0116】

(Embodiment 9)

Embodiment 9 implements a coding apparatus comprising any one of the MIL apparatuses according to Embodiment 1 to Embodiment 4, or a MIL apparatus that combines Embodiment 1 to Embodiment 4, a transmission data coding apparatus and a transmission data length adjusting apparatus.

【0117】

Next, the coding apparatus according to the present embodiment will be described referring to the FIG 11. FIG 11 is a block diagram showing a configuration of a coding apparatus according to Embodiment 9 of the present invention. As shown in FIG 11, the coding apparatus according to this embodiment is mainly configured by data generation apparatus 1101 such as a microphone, coding apparatus 1102 that performs CRC coding and error correction coding, inter-frame MIL apparatus 1103 that performs MIL between frames, rate matching apparatus 1104a and rate matching apparatus 1104b that perform transmission data repetition/puncturing and in-frame MIL apparatus 1105a and in-frame MIL apparatus 1105b that perform MIL inside a frame.

【0118】

Data generation apparatus 1101 generates data corresponding to a few frames (here 2 frames). Coding apparatus 1102 performs CRC coding and error correction coding on the 2-frame data generated.

【0119】

Inter-frame MIL apparatus 1103 performs inter-frame MIL processing on the coded 2-frame data. As the inter-frame MIL apparatus, for example, the MIL apparatus according to Embodiment 3 or Embodiment 4 above can be used.

【0120】

Rate matching apparatus 1104a and rate matching apparatus 1104b each

perform repetition/puncturing processing on data of each frame subjected to inter-frame MIL processing.

【0121】

In-frame MIL apparatus 1105a and in-frame MIL apparatus 1105b each perform in-frame MIL on data of each frame subjected to repetition/puncturing processing. As the in-frame MIL apparatus, for example, the MIL apparatus according to Embodiment 1 or Embodiment 2 above can be used.

【0122】

As shown above, this embodiment can drastically reduce the amount of memory required for the inter-frame MIL apparatuses and in-frame MIL apparatuses, and therefore can significantly reduce the circuit scale of the coding apparatus.

【0123】

(Embodiment 10)

Embodiment 10 implements a decoding apparatus comprising any one of the De-MIL apparatuses according to Embodiment 5 to Embodiment 8, or a De-MIL apparatus that combines Embodiment 5 to Embodiment 8, a reception data decoding apparatus and a reception data length adjusting apparatus.

【0124】

Next, the decoding apparatus according to the present embodiment will be described referring to the FIG 12. FIG 12 is a block diagram showing a configuration of a decoding apparatus according to Embodiment 10 of the present invention. As shown in FIG 12, the decoding apparatus according to this embodiment is mainly configured by in-frame De-MIL apparatus 1201a and De-MIL apparatus 1201b that perform De-MIL inside a frame, rate matching apparatus 1202a and rate matching apparatus 1202b that perform reception data repetition/puncturing, inter-frame De-MIL apparatus 1203 that performs De-MIL between frames, decoding apparatus 1204 that performs CRC decoding and

error correction decoding and data output apparatus 1205.

【0125】

In-frame De-MIL apparatus 1201a and in-frame De-MIL apparatus 1201b each perform in-frame De-MIL on reception data corresponding to a few frames (here 2 frames). As the in-frame De-MIL apparatus, for example, the De-MIL apparatus according to Embodiment 5 or Embodiment 6 above can be used.

【0126】

Rate matching apparatus 1202a and rate matching apparatus 1202b each perform rate matching processing on reception data subjected to De-MIL processing for each frame.

【0127】

Inter-frame De-MIL apparatus 1203 performs inter-frame MIL processing on the 2-frame reception data subjected to rate matching processing. As the inter-frame De-MIL apparatus, for example, the De-MIL apparatus according to Embodiment 7 or Embodiment 8 above can be used.

【0128】

Decoding apparatus 1204 performs error correction decoding and CRC decoding on the reception data subjected to inter-frame De-Mil processing. Data output apparatus 1205 performs output processing on the reception data subjected to error correction decoding and CRC decoding.

【0129】

As shown above, this embodiment can drastically reduce the amount of memory required for the inter-frame De-MIL apparatuses and in-frame De-MIL apparatuses, and therefore can significantly reduce the circuit scale of the coding apparatus.

【0130】

(Embodiment 11)

Embodiment 11 implements a mobile station apparatus using the coding

apparatus in Embodiment 9 and decoding apparatus in Embodiment 10. Next, the mobile station apparatus according to the present embodiment will be described referring to the FIG 13. FIG 13 is a block diagram showing the configuration of the mobile station apparatus according to Embodiment 11 of the present invention.

【0131】

As shown in FIG 13, the mobile station apparatus according to this embodiment is mainly configured by transmission/reception apparatus 1301 that performs transmission/reception processing, synchronization/demodulation apparatus 1302 that performs synchronization and demodulation processing of reception data, decoding processing apparatus 1303 according to Embodiment 10 above, data output apparatus 1304 that outputs data, data generation apparatus 1305 that generates data or captures data such as voice from the outside, coding processing apparatus 1306 in Embodiment 9 above and spreading/modulation apparatus 1307 that performs spreading/modulation processing of transmission data.

【0132】

This embodiment can drastically reduce the amount of memory required for inter-frame MIL, inter-frame De-MIL and in-frame MIL and in-frame De-MIL, and therefore can drastically reduce the circuit scale of the mobile station apparatus.

【0133】

Furthermore, in the case where the in-frame MIL apparatus in Embodiment 1 (2) is used as the in-frame MIL apparatus in coding processing apparatus 1306 and the in-frame De-MIL apparatus in Embodiment 6 (5) is used as the in-frame De-MIL apparatus in decoding processing apparatus 1303, the in-frame MIL apparatus and in-frame De-MIL apparatus can use common row patterns and column patterns, making it possible to further reduce the circuit scale.

【0134】

(Embodiment 12)

Embodiment 12 implements a base station apparatus using the coding apparatus in Embodiment 9 and decoding apparatus in Embodiment 10. Next, the base station apparatus according to the present embodiment will be described referring to the FIG 14. FIG 14 is a block diagram showing the configuration of a base station apparatus according to Embodiment 12 of the present invention.

【0135】

As shown in FIG 14, the base station apparatus according to this embodiment is mainly configured by transmission/reception apparatus 1401 that performs transmission/reception processing, demodulation apparatus 1402 that performs demodulation processing of reception data, decoding processing apparatus 1403 in Embodiment 10 above, data output apparatus 1404 that outputs data, data generation apparatus 1405 that generates data, coding processing apparatus 1406 in Embodiment 9 above and spreading/modulation apparatus 1407 that performs spreading/modulation processing of transmission data.

【0136】

As shown above, this embodiment can drastically reduce the amount of memory required for inter-frame MIL, inter-frame De-MIL and in-frame MIL and in-frame De-MIL, and therefore can drastically reduce the circuit scale of the mobile station apparatus.

【0137】

Furthermore, in the case where the in-frame MIL apparatus in Embodiment 1 (2) is used as the in-frame MIL apparatus in coding processing apparatus 1406 and the in-frame De-MIL apparatus in Embodiment 6 (5) is used as the in-frame De-MIL apparatus in decoding processing apparatus 1403, the in-frame MIL apparatus and in-frame De-MIL apparatus can use common row patterns and

column patterns, making it possible to further reduce the circuit scale.

【0138】

The above embodiment describes the case where at least one element of stage 1 of a MIL expression are used, but the present invention is also applicable to a case where at least one element of any stage are used.

【0139】

The above embodiment describes the case where when the sequence of data is rearranged between frames, a column pattern developed from a MIL expression of stage 1 included in the MIL expression is used, but the present invention is also applicable to a case where a row pattern developed from a MIL expression of stage 1 included in the MIL expression is used.

【0140】

Furthermore, the above embodiment describes the case where when the sequence of data is rearranged between frames, a MIL pattern developed from a MIL expression of stage 1 included in the MIL expression is used, but the present invention is also applicable to a case where when one MIL expression included in a MIL expression is lower than the other MIL expression in the MIL expression by at least one stage, the MIL pattern developed from the other MIL expression is used.

【0141】

[EFFECT OF THE INVENTION]

As described above, the present invention creates at least one MIL pattern (sequence conversion series) using any element included in a MIL expression(sequence conversion rule expression) stipulated for every input data item and changes the sequence of the input data using the created MIL pattern, and therefore can provide an interleave apparatus capable of reducing the amount of memory required.

[BRIEF DESCRIPTION OF DRAWINGS]

[FIG 1]

A block diagram showing the configuration of an MIL apparatus according to Embodiment 1 of the present invention;

[FIG 2]

A flow chart showing processing of writing to an output memory by an address calculation apparatus in the MIL apparatus according to Embodiment 1 of the present invention;

[FIG 3]

An amount of memory required of the MIL apparatus according to Embodiment 1 above compared to the conventional system;

[FIG 4]

A flow chart showing processing of writing to an output memory by an address calculation apparatus in the MIL apparatus according to Embodiment 2 of the present invention;

[FIG 5]

A flow chart showing processing of writing to an output memory by an address calculation apparatus in the MIL apparatus according to Embodiment 3 of the present invention;

[FIG 6]

A flow chart showing processing of writing to an output memory by an address calculation apparatus in the MIL apparatus according to Embodiment 4 of the present invention;

[FIG 7]

A flow chart showing processing of writing to an output memory by an address calculation apparatus in the De-MIL apparatus according to Embodiment 5 of the present invention;

[FIG 8]

A flow chart showing processing of writing to an output memory by an

address calculation apparatus in the De-MIL apparatus according to Embodiment 6 of the present invention;

[FIG 9]

A flow chart showing processing of writing to an output memory by an address calculation apparatus in the De-MIL apparatus according to Embodiment 7 of the present invention;

[FIG 10]

A flow chart showing processing of writing to an output memory by an address calculation apparatus in the De-MIL apparatus according to Embodiment 8 of the present invention;

[FIG 11]

A block diagram illustrating a configuration of a coding apparatus according to the Embodiment 9 of the present invention;

[FIG 12]

A block diagram illustrating a configuration of a decoding apparatus according to the Embodiment 10 of the present invention;

[FIG 13]

A block diagram showing the configuration of a mobile station apparatus according to Embodiment 11 of the present invention;

[FIG 14]

A block diagram showing a configuration of a base station apparatus according to Embodiment 12 of the present invention;

[FIG 15]

A block diagram showing a configuration of a conventional MIL apparatus; and

[FIG 16]

A flow chart showing an operation of a conventional MIL apparatus; and

[EXPLANATIONS OF LETTERS OR NUMERALS]

101	INPUT MEMORY
102	ROW PATTERN MEMORY
103	COLUMN PATTERN MEMORY
104	OUTPUT MEMORY
105	ADDRESS CALCULATION APPARATUS

[NAME OF DOCUMENT] ABSTRACT

[ABSTRACT]

[OBJECT] To provide an interleave apparatus that reduces the amount of memory required;

[OVERCOMING MEANS] Input memory 101 stores input data. Row pattern memory 102 stores row patterns. Column pattern memory 103 stores column patterns. Output memory 104 stores output data with the sequence of the input data rearranged. Address calculation apparatus 105 calculates addresses of the input data to be written to the output data and further writes input data read from input memory 101 in output memory 104 as output data based on the calculated input addresses.

[SELECTED DRAWING] FIG 1

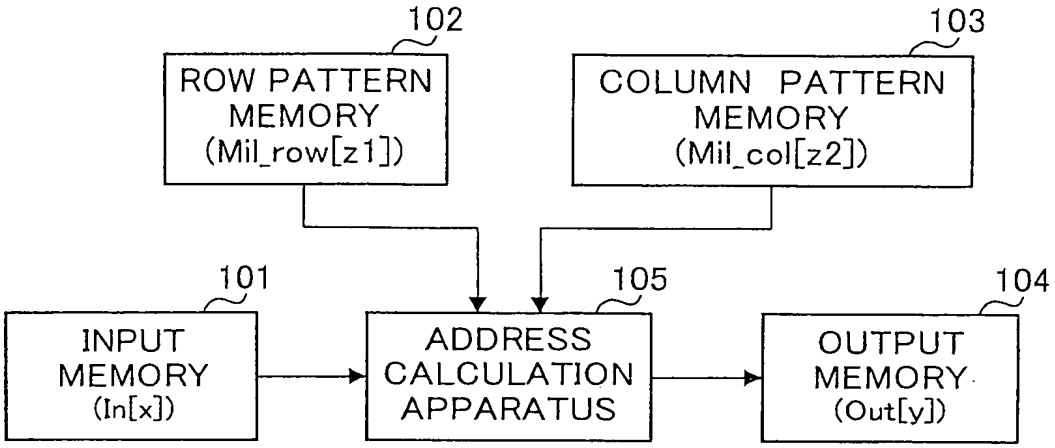

FIG.1

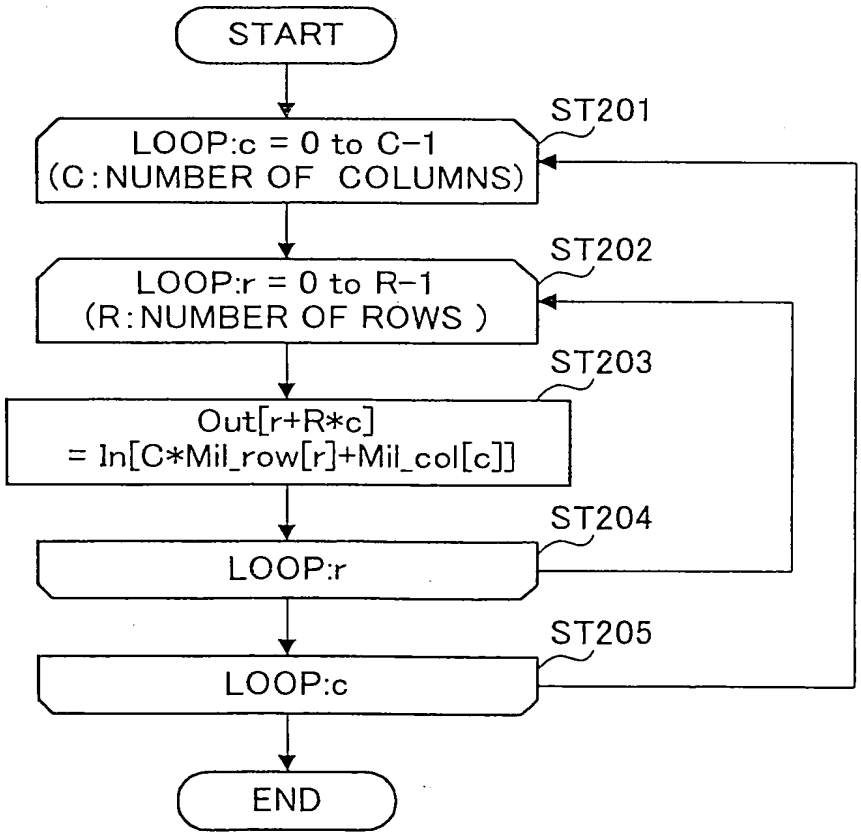

FIG.2

MIL PATTERN	MIL IMPLEMENTATION METHOD	AMOUNT OF MEMORY(WORD) *EXCEPT INPUT/ OUTPUT MEMORY	RATIO WHEN CONVERTIONAL METHOD IS ASSUMED 100
①	CONVENTIONAL METHOD	320	100.00
	PROPOSED METHOD	36	11.25
②	CONVENTIONAL METHOD	81376	100.00
	PROPOSED METHOD	5102	6.27

FIG.3

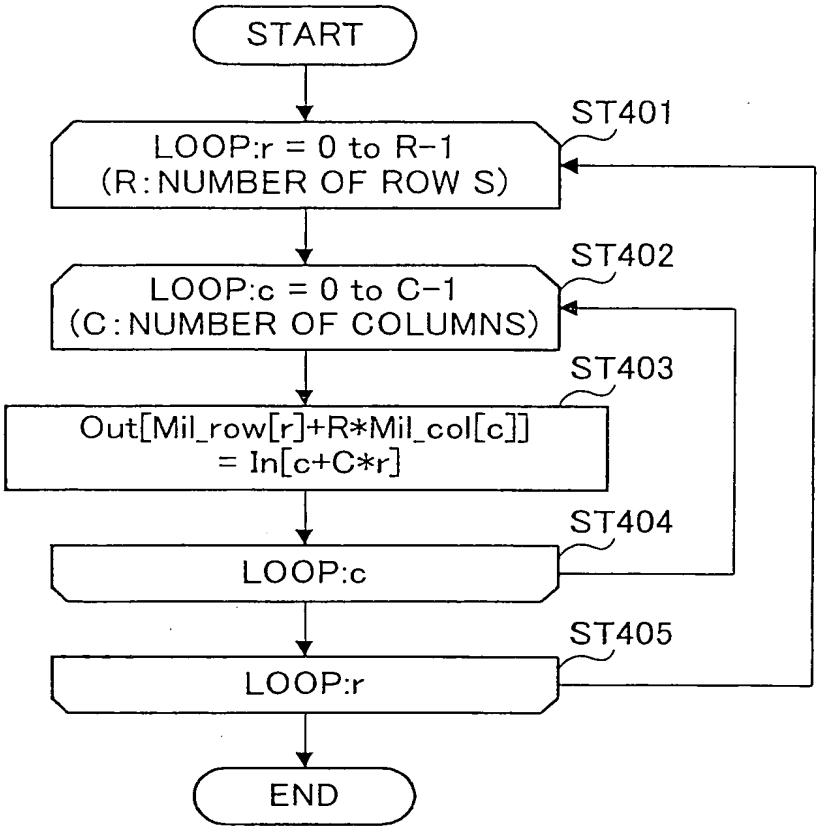
START
ST401
LOOP:r = 0 to R-1
(R:NUMBER OF ROW S)
ST402
LOOP:c = 0 to C-1
(C:NUMBER OF COLUMNS)
ST403
Out[Mil_row[r]+R*Mil_col[c]]
= In[c+C*r]
ST404
LOOP:c
ST405
LOOP:r
END

FIG.4

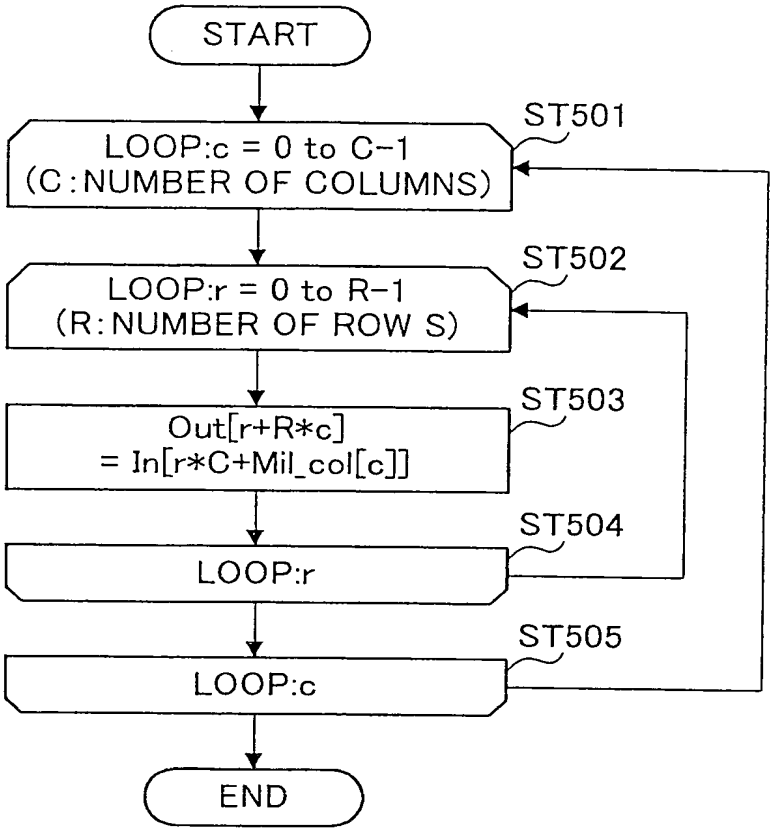
START
ST501
LOOP:c = 0 to C-1
(C:NUMBER OF COLUMNS)
ST502
LOOP:r = 0 to R-1
(R:NUMBER OF ROW S)
ST503
Out[r+R*c]
= In[r*C+Mil_col[c]]
ST504
LOOP:r
ST505
LOOP:c
END

FIG.5

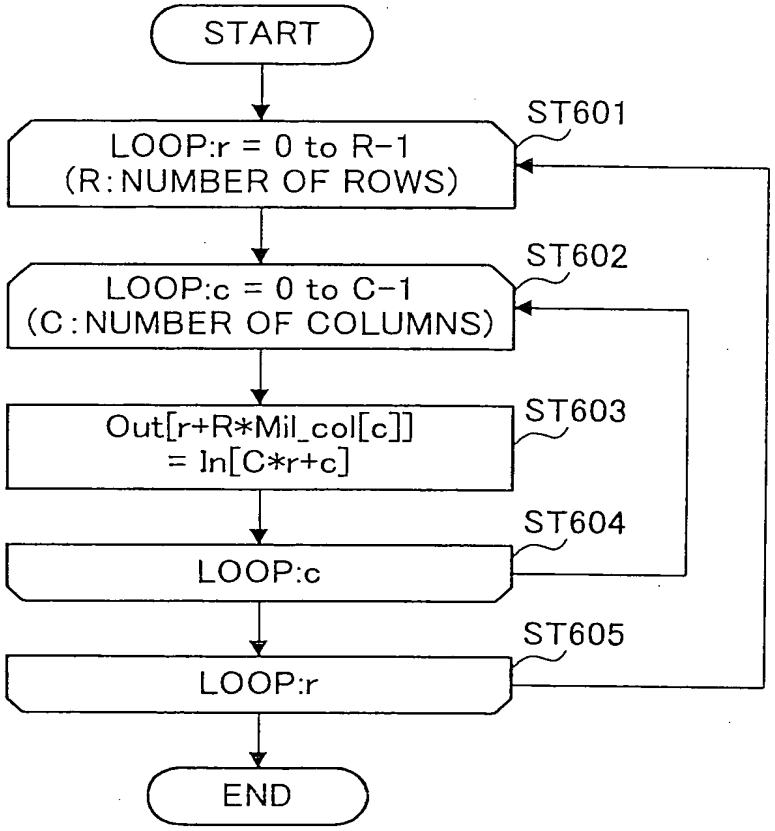
START
ST601
LOOP:r = 0 to R-1
(R:NUMBER OF ROWS)
ST602
LOOP:c = 0 to C-1
(C:NUMBER OF COLUMNS)
ST603
Out[r+R*Mil_col[c]]
= In[C*r+c]
ST604
LOOP:c
ST605
LOOP:r
END

FIG.6

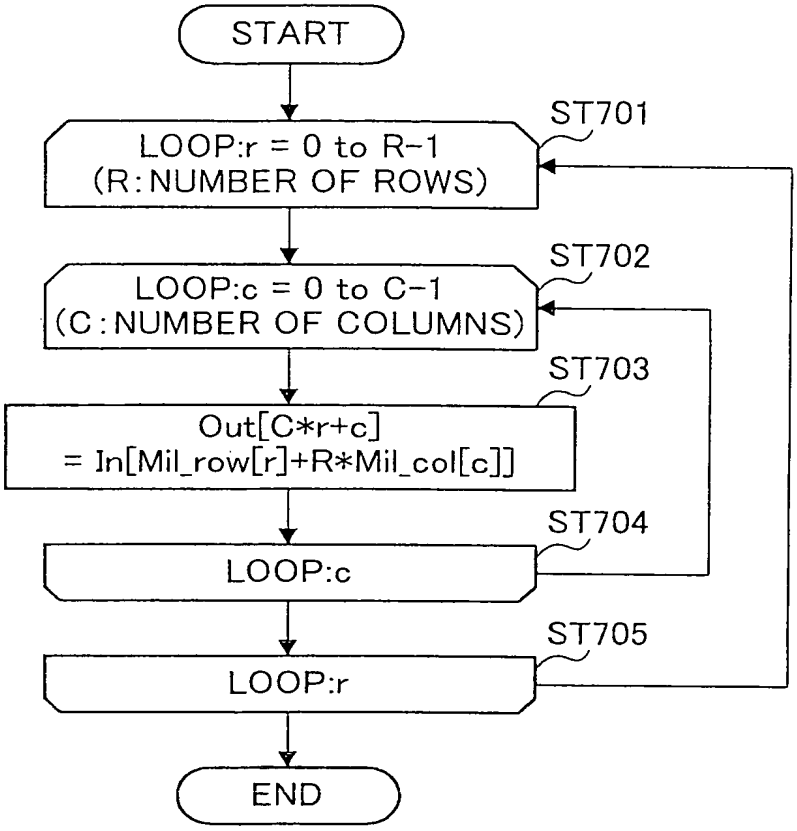
START
ST701
LOOP:r = 0 to R-1
(R:NUMBER OF ROWS)
ST702
LOOP:c = 0 to C-1
(C:NUMBER OF COLUMNS)
ST703
Out[C*r+c]
= In[Mil_row[r]+R*Mil_col[c]]
ST704
LOOP:c
ST705
LOOP:r
END

FIG.7

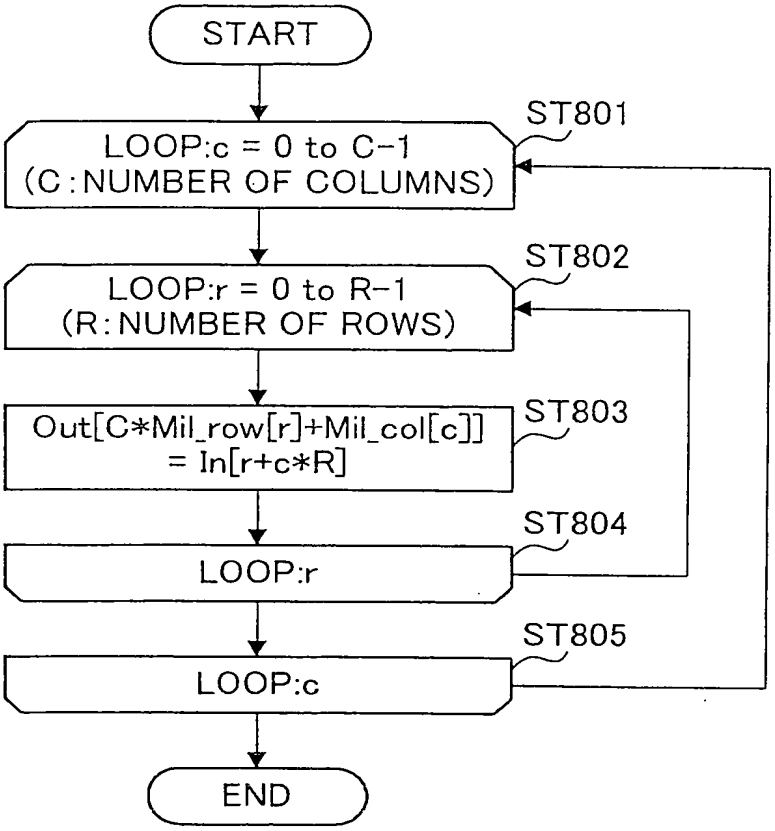
START
ST801
LOOP:c = 0 to C-1
(C : NUMBER OF COLUMNS)
ST802
LOOP:r = 0 to R-1
(R : NUMBER OF ROWS)
ST803
Out[C*Mil_row[r]+Mil_col[c]]
= In[r+c*R]
ST804
LOOP:r
ST805
LOOP:c
END

FIG. 8

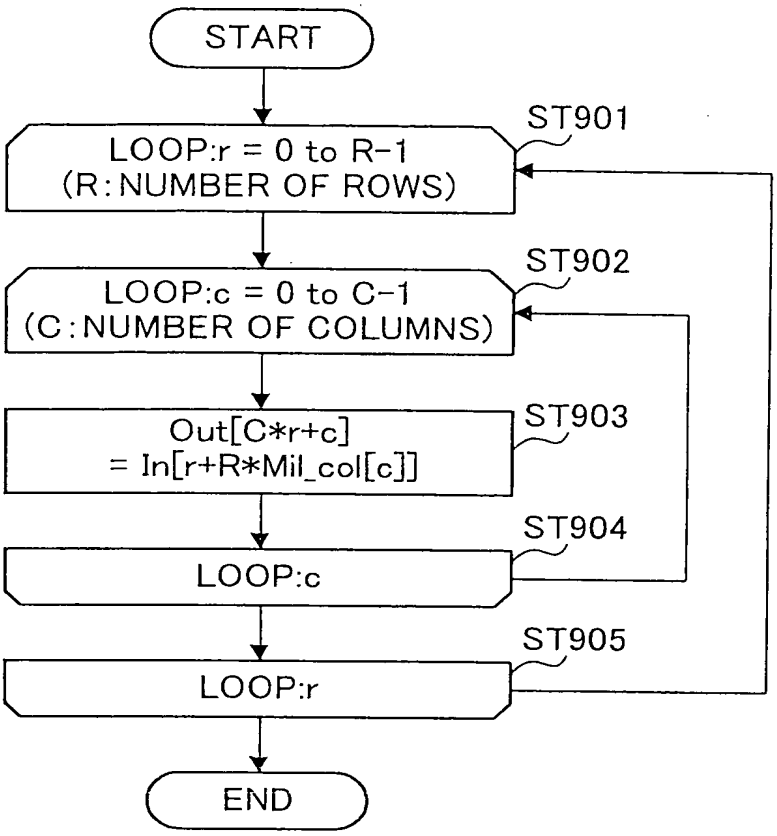
START
ST901
LOOP:r = 0 to R-1
(R:NUMBER OF ROWS)
ST902
LOOP:c = 0 to C-1
(C:NUMBER OF COLUMNS)
ST903
Out[C*r+c]
= In[r+R*Mil_col[c]]
ST904
LOOP:c
ST905
LOOP:r
END

FIG. 9

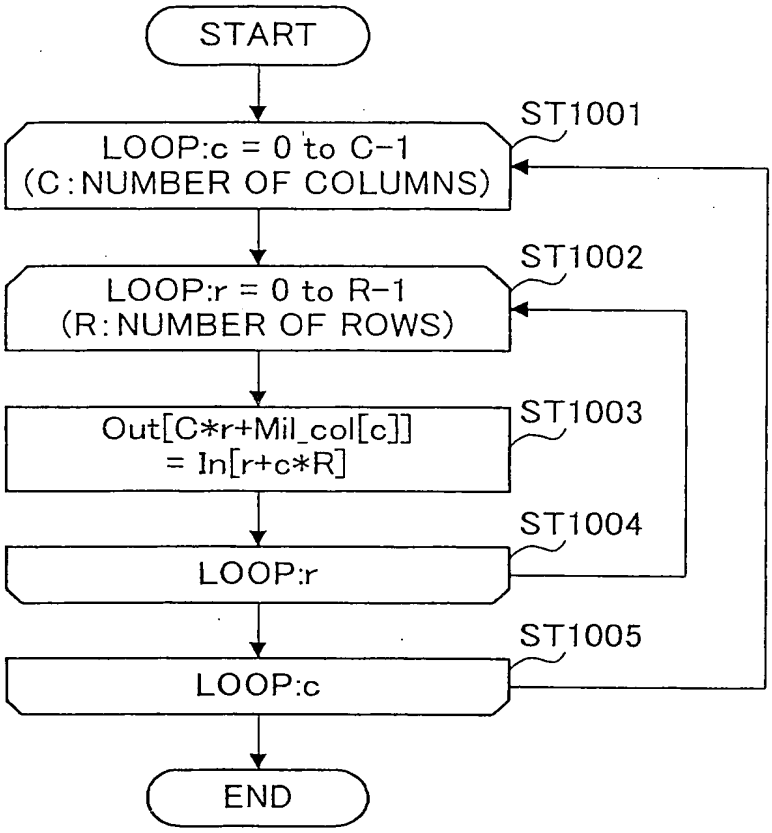
START
ST1001
LOOP:c = 0 to C-1
(C:NUMBER OF COLUMNS)
ST1002
LOOP:r = 0 to R-1
(R:NUMBER OF ROWS)
ST1003
Out[C*r+Mil_col[c]]
= In[r+c*R]
ST1004
LOOP:r
ST1005
LOOP:c
END

FIG. 10

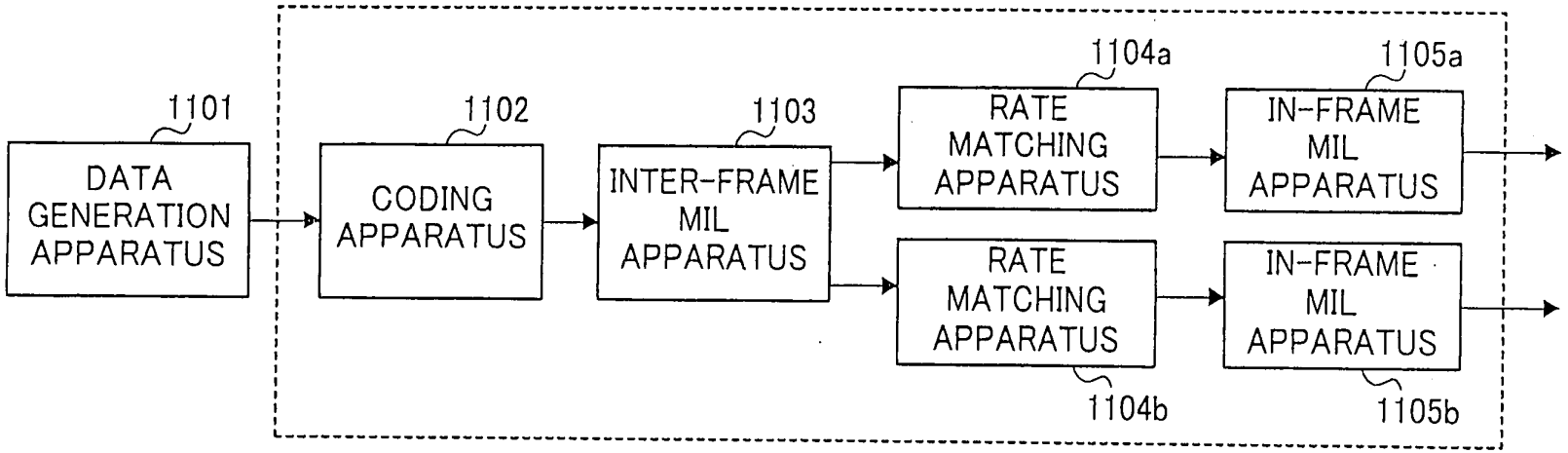
1101
DATA GENERATION APPARATUS
1102
CODING APPARATUS
1103
INTER-FRAME MIL APPARATUS
1104a
RATE MATCHING APPARATUS
1105a
IN-FRAME MIL APPARATUS
RATE MATCHING APPARATUS
1104b
IN-FRAME MIL APPARATUS
1105b

FIG.11

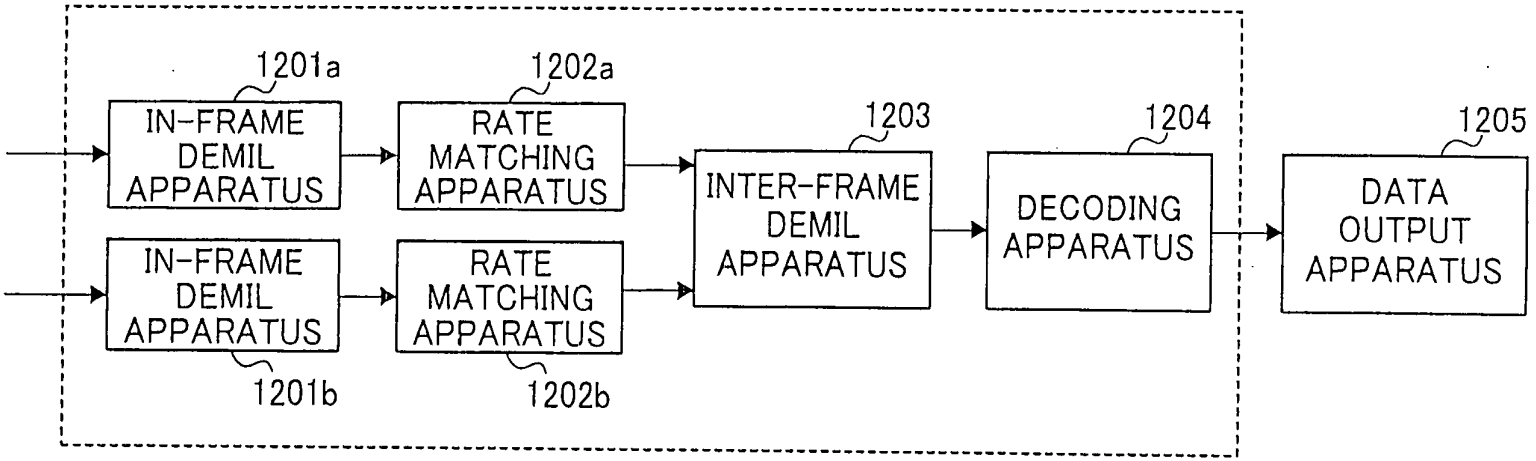
1201a
1202a
1203
1204
1205
IN-FRAME DEMIL APPARATUS
RATE MATCHING APPARATUS
INTER-FRAME DEMIL APPARATUS
DECODING APPARATUS
DATA OUTPUT APPARATUS
IN-FRAME DEMIL APPARATUS
RATE MATCHING APPARATUS
1201b
1202b

FIG. 12

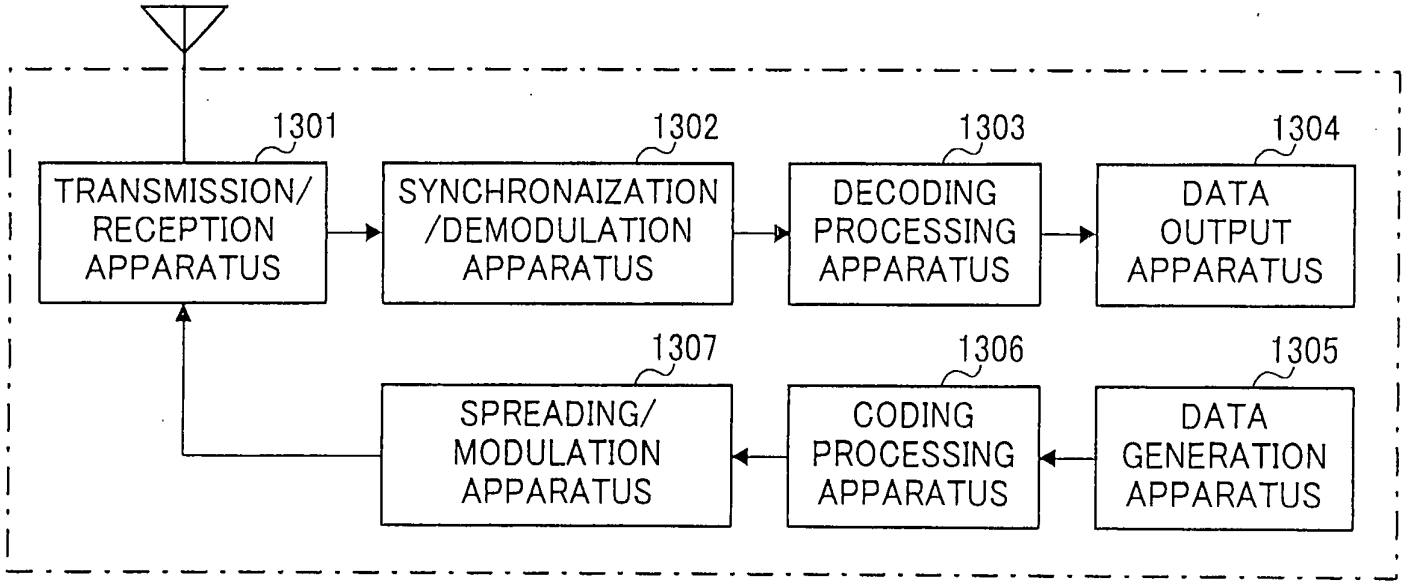
1301
TRANSMISSION/
RECEPTION
APPARATUS
1302
SYNCHRONAIZATION
/DEMODULATION
APPARATUS
1303
DECODING
PROCESSING
APPARATUS
1304
DATA
OUTPUT
APPARATUS
1307
SPREADING/
MODULATION
APPARATUS
1306
CODING
PROCESSING
APPARATUS
1305
DATA
GENERATION
APPARATUS
MOBILE APPARATUS

FIG.13

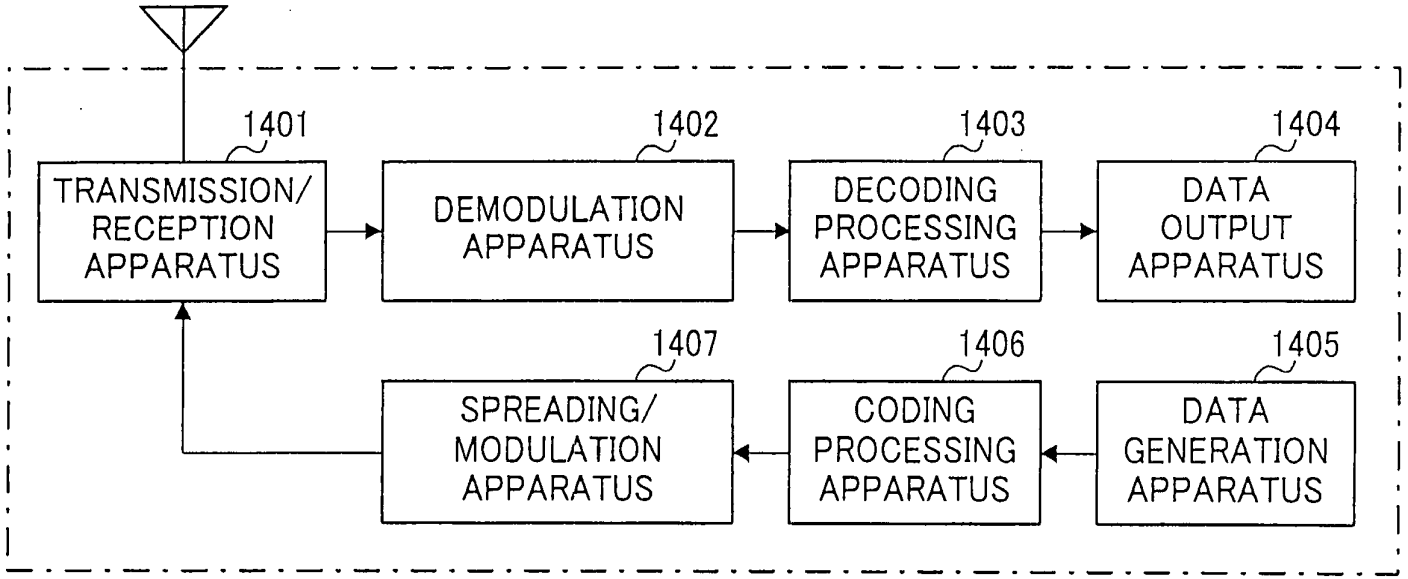
1401
TRANSMISSION/ RECEPTION APPARATUS
1402
DEMODULATION APPARATUS
1403
DECODING PROCESSING APPARATUS
1404
DATA OUTPUT APPARATUS
1407
SPREADING/ MODULATION APPARATUS
1406
CODING PROCESSING APPARATUS
1405
DATA GENERATION APPARATUS
BASE STATION

FIG. 14

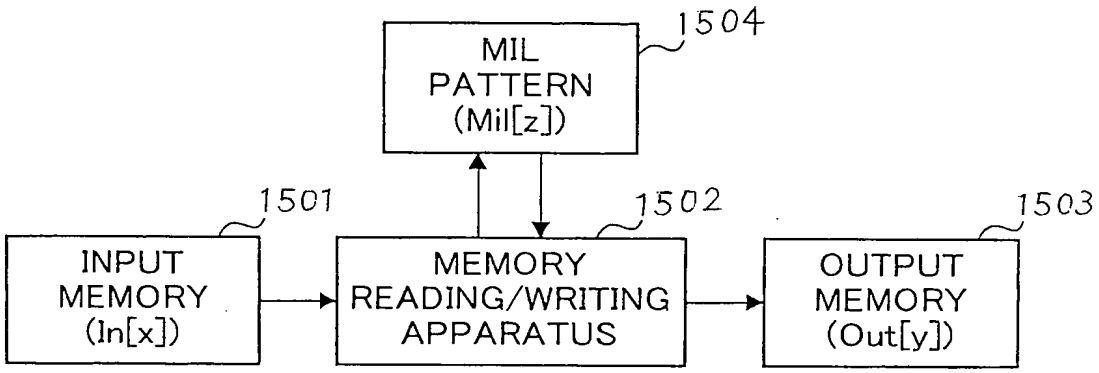
MIL
PATTERN
(Mil[z])
1504
1501
1502
1503
INPUT
MEMORY
(In[x])
MEMORY
READING/WRITING
APPARATUS
OUTPUT
MEMORY
(Out[y])

FIG. 15

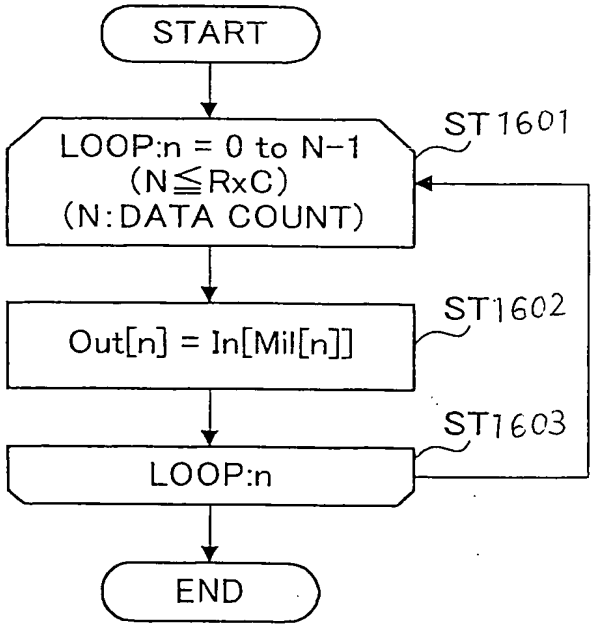
START
LOOP:n = 0 to N-1
(N≦RxC)
(N:DATA COUNT)
ST1601
Out[n] = In[Mil[n]]
ST1602
LOOP:n
ST1603
END

FIG. 16